Topic 9

JTAG Boundary-Scan

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(Based on Ben Bennetts' Tutorial)

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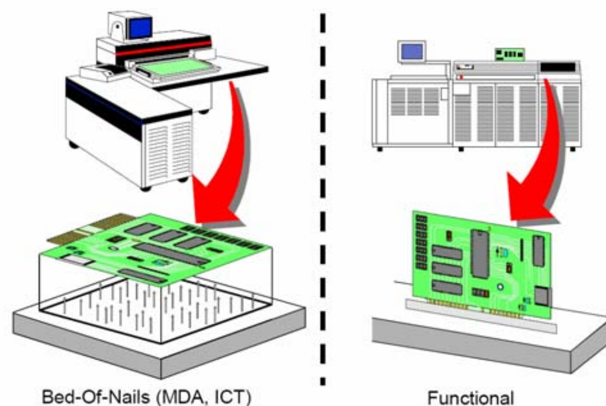
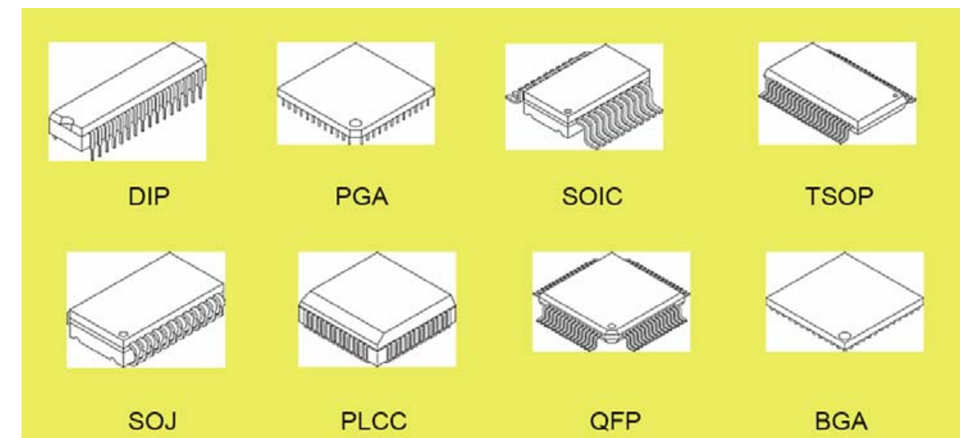
Sources & Background

- JTAG Boundary Scan is from IEEE Standard 1149.1
- Most of slides here are based on the document "Boundary Scan Tutorial" by Ben Bennetts, for ASSET InterTech Inc., ww.asset-intertech.com/pdfs/boundaryscan_tutorial.pdf

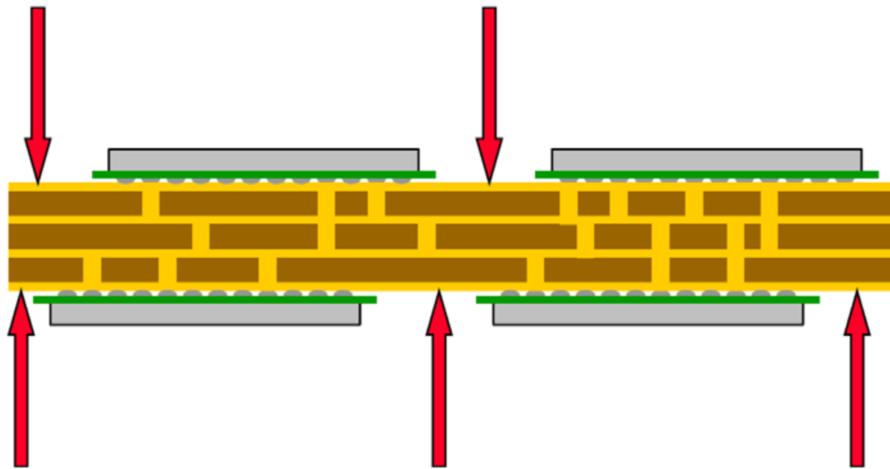
The old way



Problem with modern packaging styles



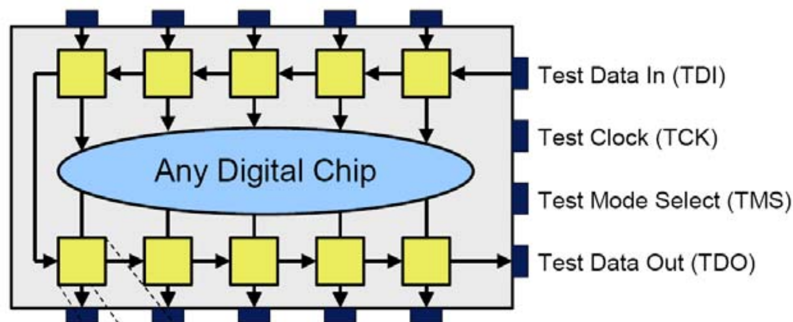
Problem with multi-layer PCB

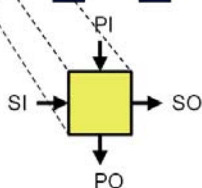


Motivation of Boundary Scan

- Basic motivation was miniaturization of device packaging, leading to …
- surface mount packaging styles, leading to …
- double sided boards, leading to …
- multi-layer boards, leading to …
- a reduction of physical access test lands for traditional bed-of-nail in-circuit testers
- Problem: how to test for manufacturing defects in the future?
- Solution: add boundary-scan registers to the devices

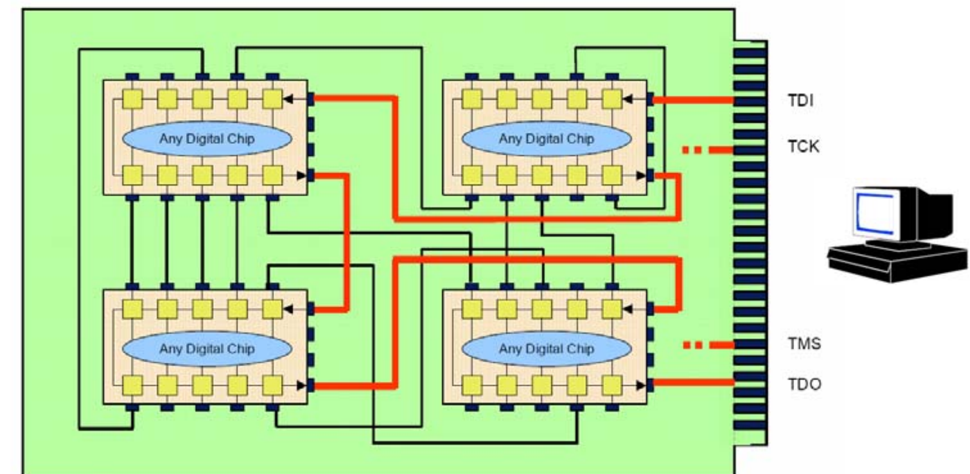
Principle of Boundary Scan



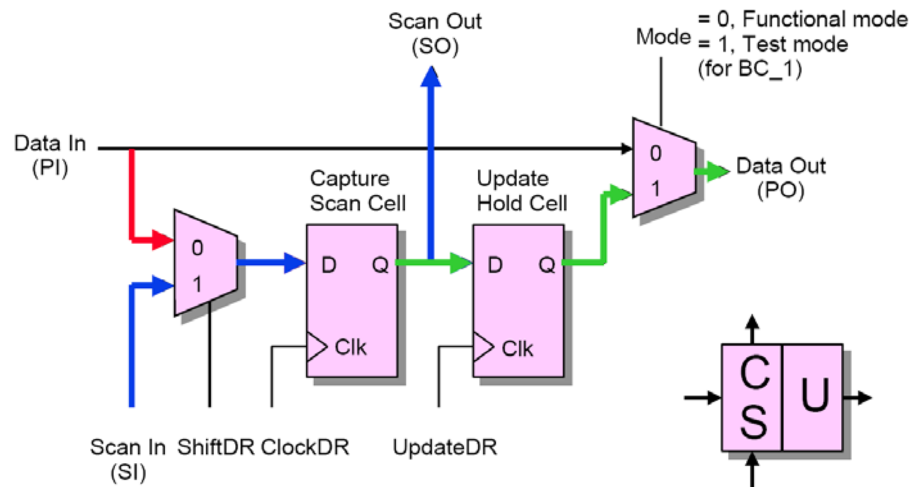


Each boundary-scan cell can:
- Capture data on its parallel input PI
- Update data onto its parallel output PO
- Serially scan data from SO to its neighbour's SI
- Behave transparently: PI passes to PO
- Note: all digital logic is contained inside the boundary-scan register

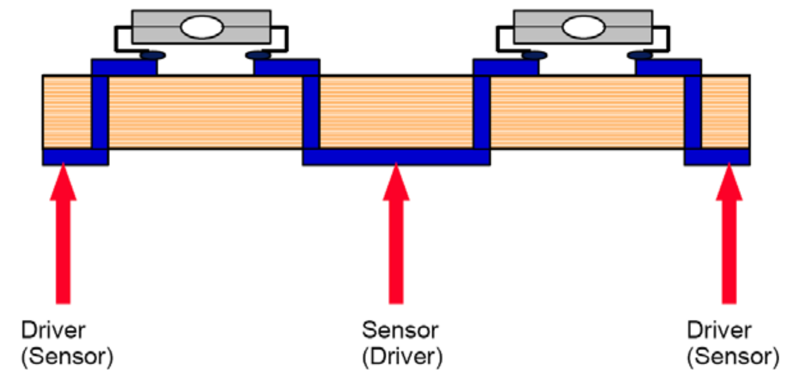
The Boundary Scan Path



Basic Boundary Scan Cell

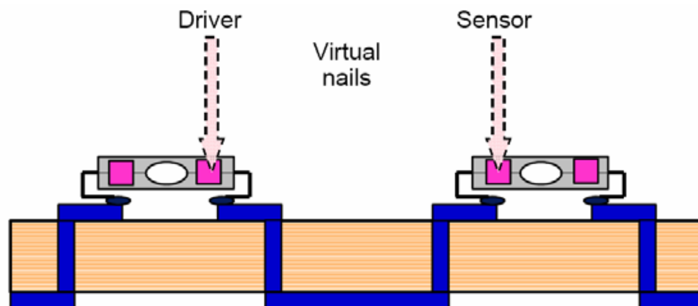


Defect Coverage: Bed-of-nails



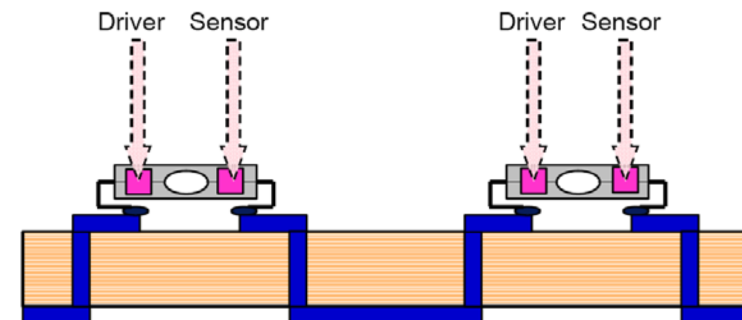
Defects covered: nail - plated-through-hole - interconnect - solder - leg - bond wire - device - bond wire - leg - solder - interconnect - plated through hole - nail

Defect Coverage: Extest



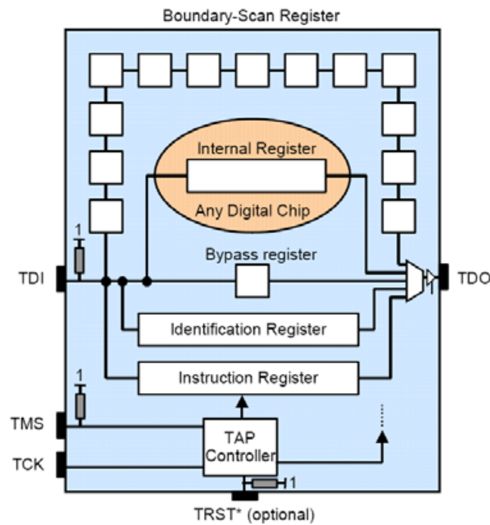
In this mode (EXternal TEST), defects covered:
driver (TX) scan cell - driver amp - bond wire - leg - solder - interconnect
- solder - leg - bond wire - driver amp - sensor (RX) scan cell

Defect Coverage: Intest

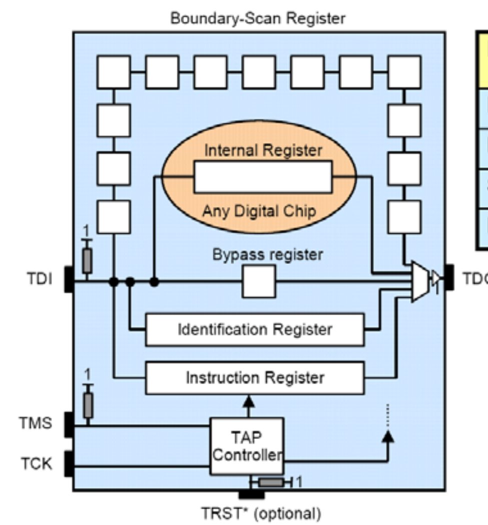


In this mode (INternal TEST), defects covered:
driver scan cell - device - sensor scan cell

1149.1 Chip Architecture



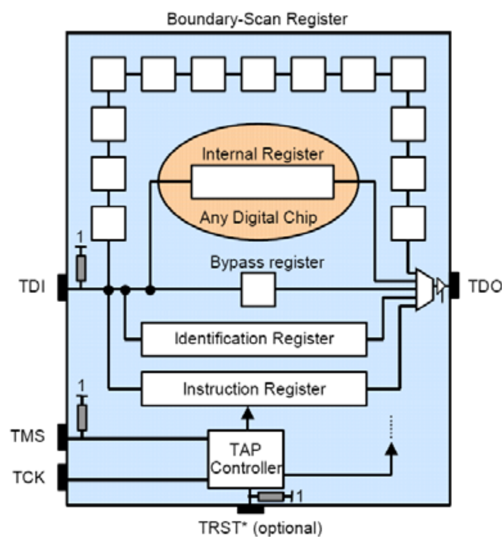
Mandatory Instructions and Reset Modes

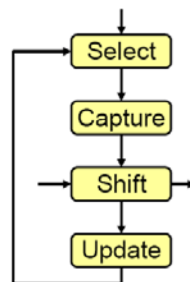


Instruction	Target (Active) Register	Code
Extest	Boundary Scan	Formerly All-0s
Bypass	Bypass	All-1s
Sample	Boundary Scan	Undefined
Preload	Boundary Scan	Undefined

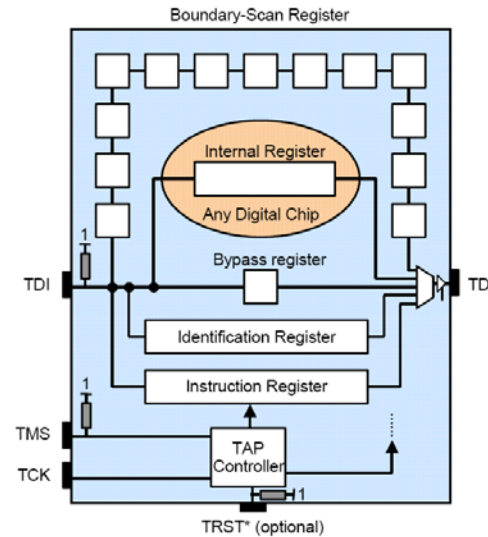
IR $\geq$ 2
Reset:
TMS = 1, 5 x TCK

Target Register Modes



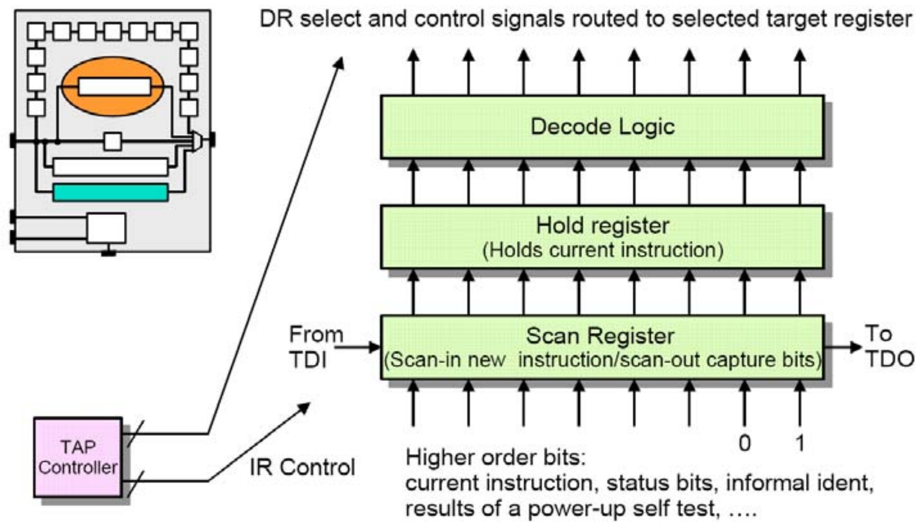


Open-Circuit TDI, TMS and TRST*?



- An open-circuit TDI, TMS or TRST* must go to logic-1. Why?
- TDI: Bypass instruction is loaded: safe instruction
- TMS: TAP controller placed into Test_Logic Reset state after 5 TCKs, max: safe state
- TRST* not asserted. Rest of 1149.1 logic still usable

Instruction Register

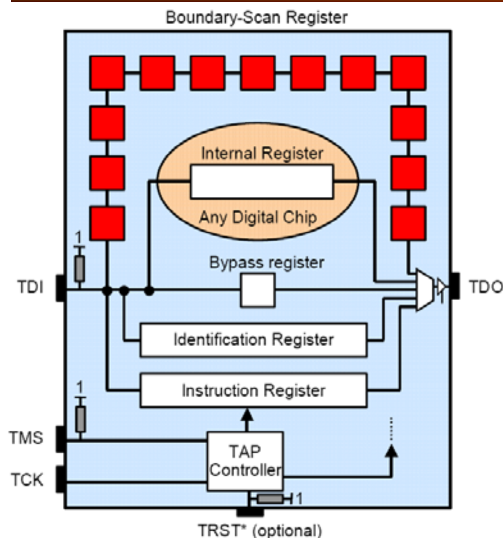


Standard Instructions

Instruction	Selected Data Register
Mandatory:	
Extest	Boundary scan (formerly all-0s code)
Bypass	Bypass (initialised state, all-1s code)
Sample	Boundary scan (device in functional mode)
Preload	Boundary scan (device in functional mode)
Optional:	
Intest	Boundary scan
Idcode	Identification (initialised state if present)
Usercode	Identification (for PLDs)
Runbist	Result register
Clamp	Bypass (output pins in safe state)
HighZ	Bypass (output pins in high-Z state)

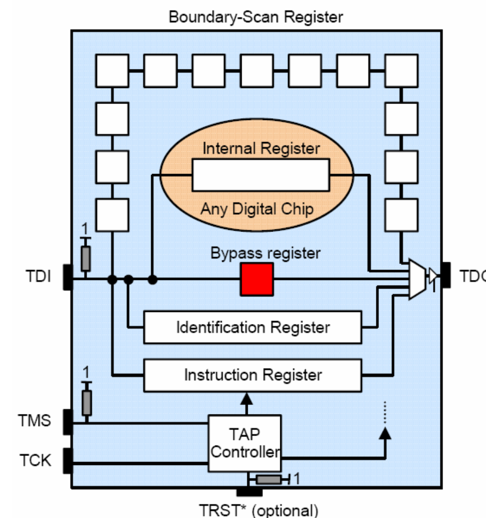
NB. All unused instruction codes must default to ***Bypass***

Extest Instructions



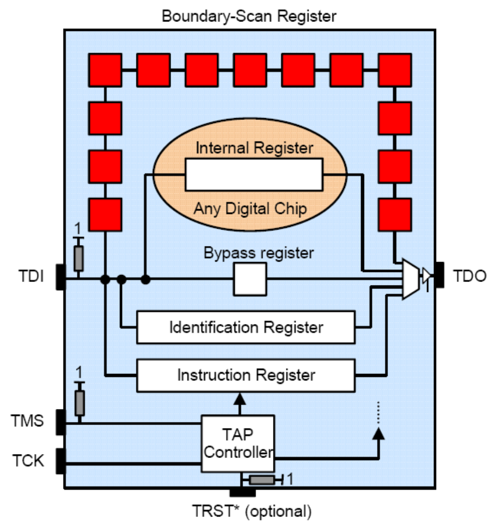
- Boundary-scan register selected
- Used to apply patterns to the interconnect structures on the board
- Boundary-scan cells have permission to write to their outputs (device in test mode)

Bypass Instruction



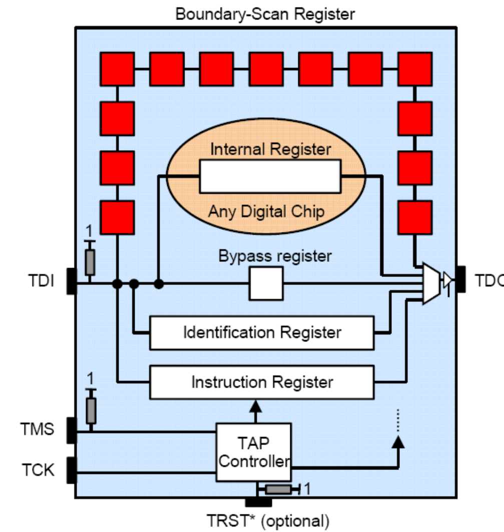
- Bypass register selected
- Used to allow quick passage through this device to another device connected in the chain

Sample and Preload Instruction



- Boundary scan register selected
- Used to Preload known values in the boundary scan cells.
- Also used to Sample (Capture) mission-mode signals into the boundary-scan cells
- Device in functional mode, not test mode

Intest Instruction



- Boundary scan register selected
- Used to apply patterns to the device itself
- Boundary scan cells have permission to write to their outputs (device in test mode)

Idcode Instruction

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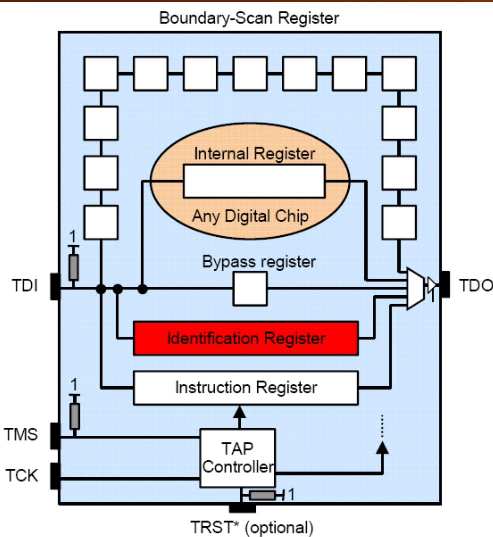

- Optional Identification register selected, if available, else Bypass register selected
- Used to capture internal 32-bit identification code (manufacturer, part number, version number) and then shift out through TDO

Usercode Instruction

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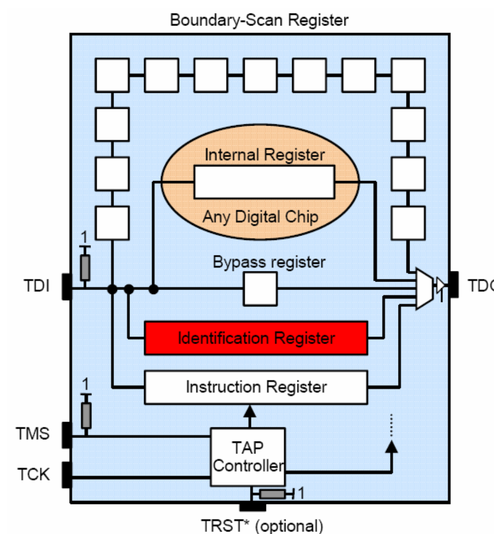
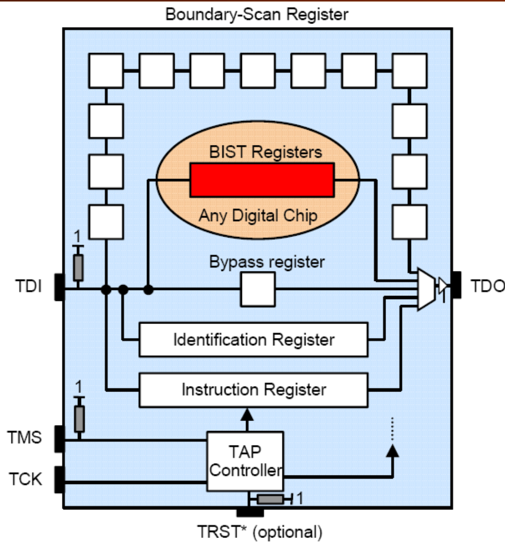


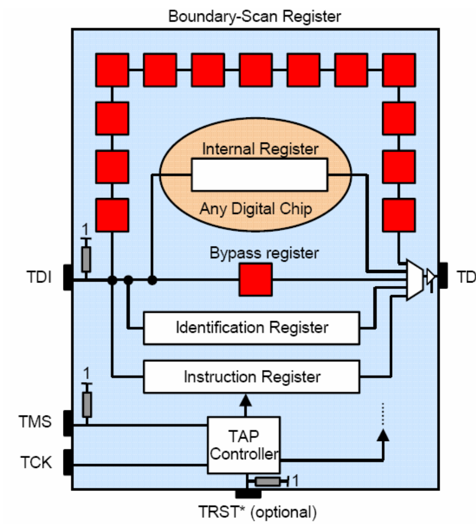
- Optional Identification register selected, if available, else Bypass register selected
- Use to capture an alternative 32-bit identification code for dual personality devices e.g. PLDs

RunBIST Instruction



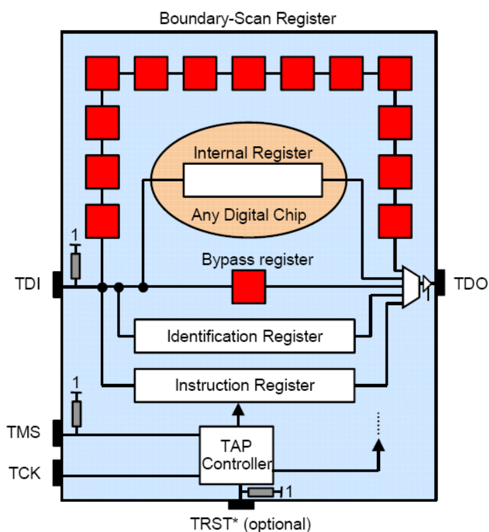
- Control registers for initiating internal BIST (Memory or Logic)
- Pass/fail register targeted as final selected register

Clamp Instruction



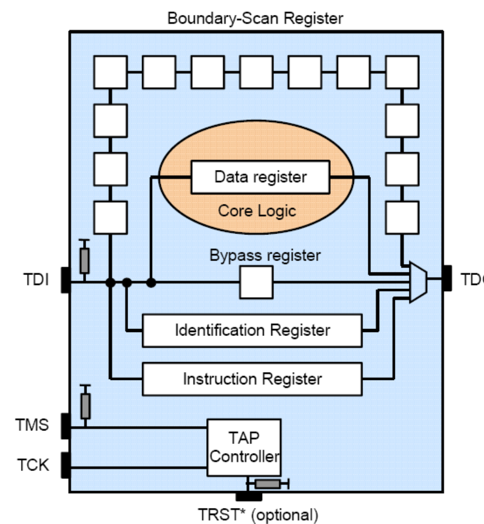
- Known values are pre-loaded into boundary scan cells using ***Preload*** instruction
- ***Clamp*** drives these values to the output pins but leaves Bypass register as the selected register

HighZ Instruction



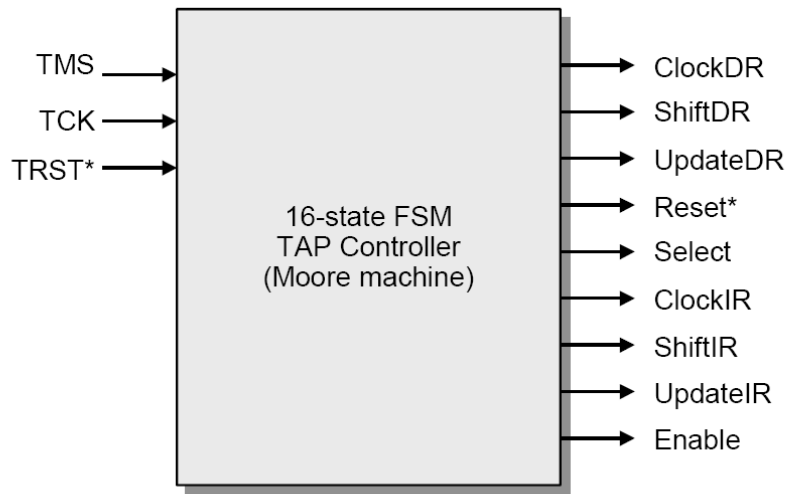
- Control-to-Z values are pre-loaded into high-Z control cells using the ***Preload*** instruction
- ***HighZ*** drives these values to the three-state controls causing them to go to their high-Z drive state but leaves Bypass register as the selected register

Test Access Port (TAP)

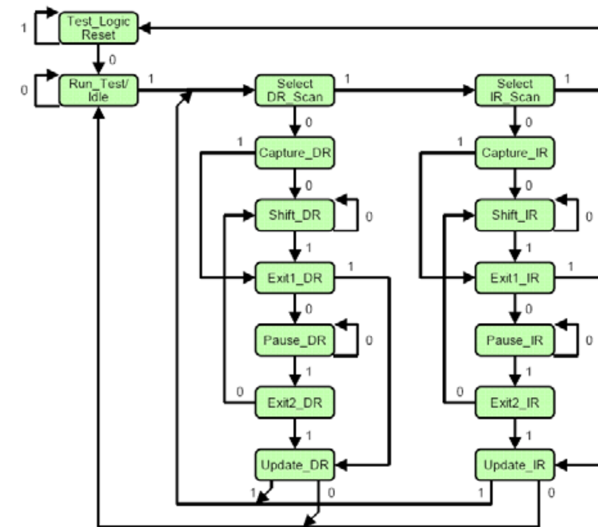


Test Data In (TDI)	Serial data in Sampled on rising edge Default = 1
Test Data Out (TDO)	Serial data out Sampled on falling edge Default = Z (only active during a shift operation)
Test Mode Select (TMS)	Input Control Sampled on rising edge Default = 1
Test Clock (TCK)	Dedicated clock Any frequency
Test Reset (TRST*)	Optional async reset Active low Default = 1

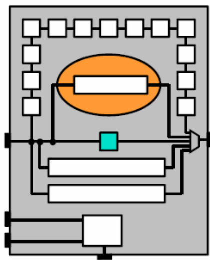
TAP Controller



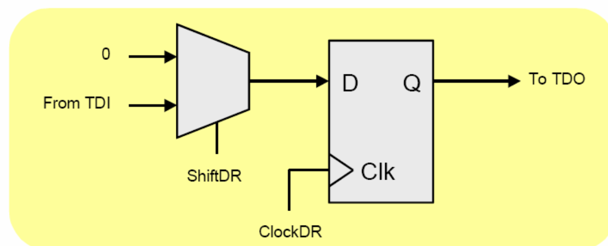
TAP Controller State Diagram



Bypass Register

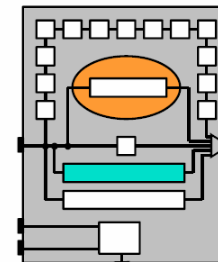


- One-bit shift register, selected by the ***Bypass*** instruction
- Captures a hard-wired 0
- Note: in the *Test-Logic/Reset* state, the Bypass register is the default register if no Identification Register present



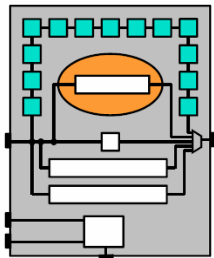
Identification Register

Identification Register



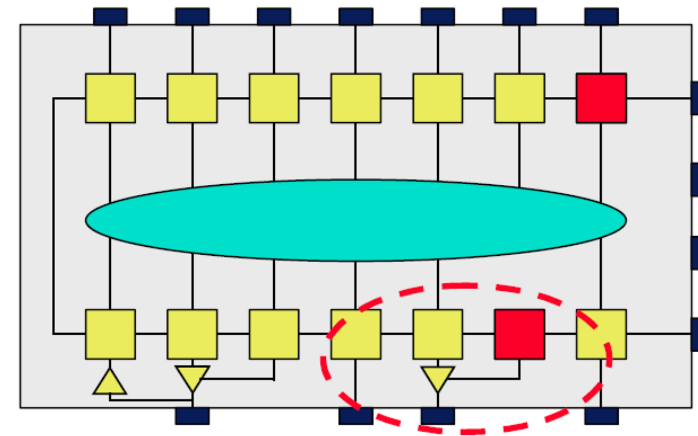
- 32-bit shift register
- Selected by ***Idcode*** and ***Usercode*** instruction
- No parallel output
- Captures a hard-wired 32-bit word
- Main function: identify device owner and part number
- Note: ***Idcode*** is power-up instruction if Identification Register is present, else ***Bypass***

Boundary Scan Register



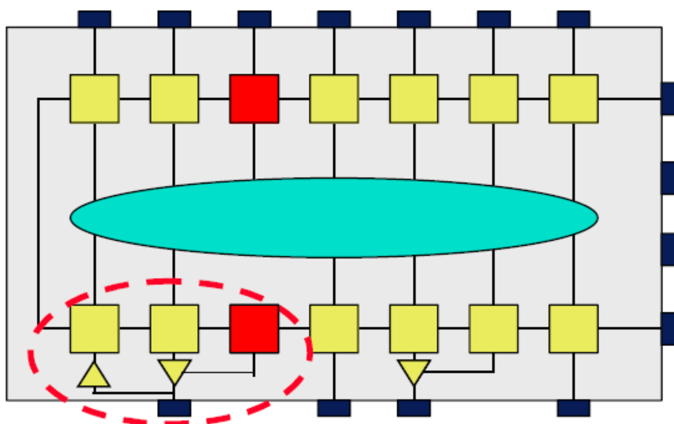
- Shift register with boundary-scan cells on:
  - device input pins
  - device output pins
  - control of three-state outputs
  - control of bidirectional cells
- Selected by the ***Extest***, ***Intest***, ***Preload*** and ***Sample*** instructions

Boundary Scan Cell OZ



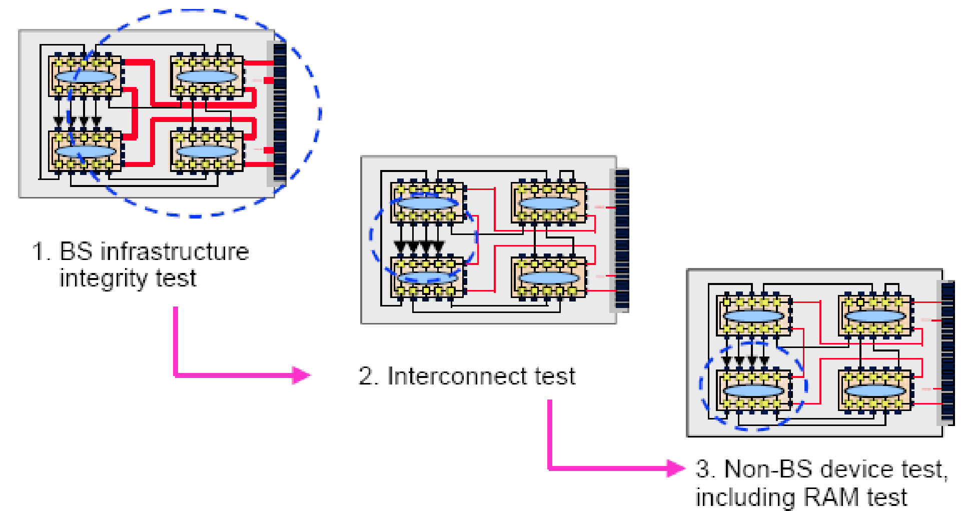
On all device signal IO, control of three-state: **dual-mode input signal** or additional scan cell

Boundary Scan Cell IO



On control of bidirectional IO: dual-mode input signal

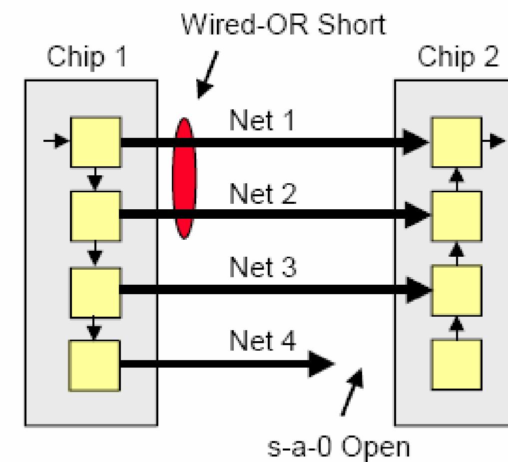
Application at Board Level



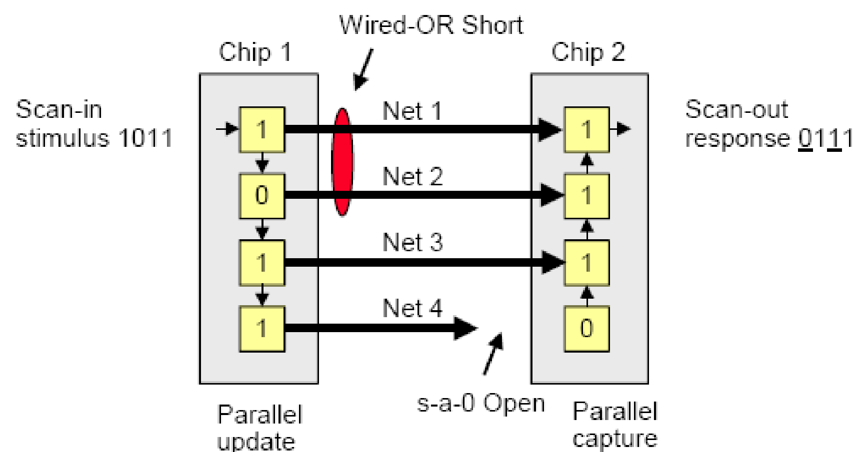
Board Defects

- Missing component, wrong component, mis-oriented component, broken track, shorted tracks, pin-to-solder open circuit, pin-to-pin solder shorts
- Number of 2-net short circuit faults between k interconnects = k(k-1)/2
- Equivalent fault models for shorts: bridging of type wired-AND and wired-OR
- Open circuits are modelled down-stream as stuck-at-1 or stuck-at-0 faults

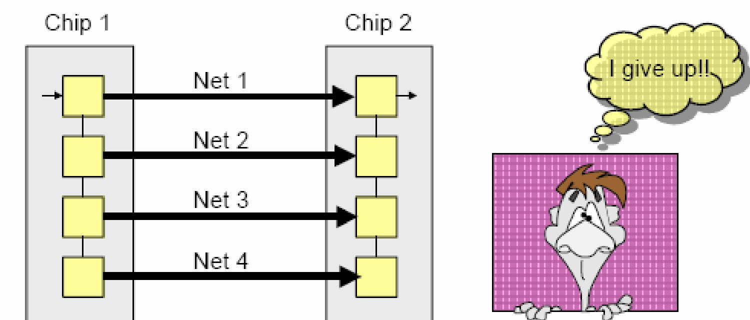
Example of faults



Generating Open and Short Test

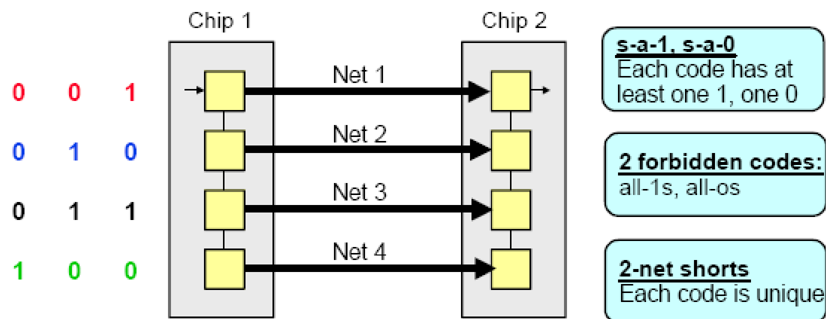


How many tests are needed?



Determine a set of tests to detect all:
- open circuits, modelled as any net s-a-1 and s-a-0, and
- short circuits, modelled as all 2-net shorts of type wired-AND and wired-OR i.e. {1,2}, {1,3}, {1,4}, {2,3}, {2,4}, {3,4}

Building the tests



Determine a set of tests to detect all:
- * open circuits, modelled as any net s-a-1 and s-a-0, and
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  i.e. {1,2}, {1,3}, {1,4}, {2,3}, {2,4}, {3,4}

Number of Tests

Number of tests

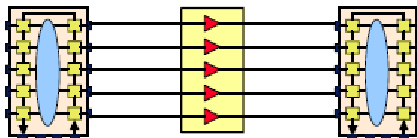
= Number of bits in the code

= ceil $\log_2(k + 2)$, k = number of interconnects

= 13 for k = 8000 interconnects

It's so simple, it's beautiful!!

Testing non-Boundary Scan cluster



- ❑ On modern boards, most non-boundary-scan devices are simple pass-thru devices e.g. line drivers
- ❑ Consequently, tests for presence, orientation and bonding are easily generated and easily applied via the embracing boundary-scan devices

Combining BS and Nails

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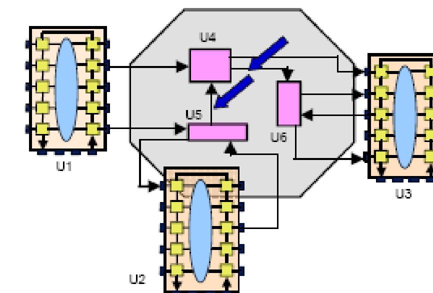
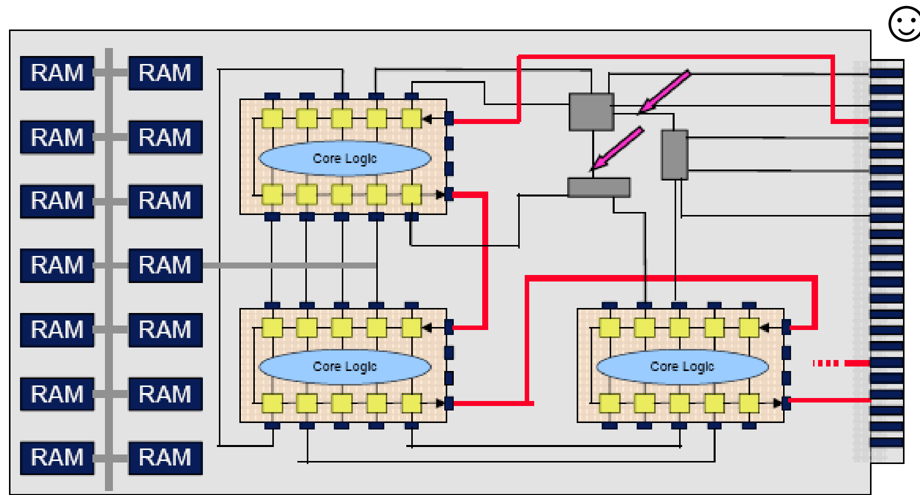
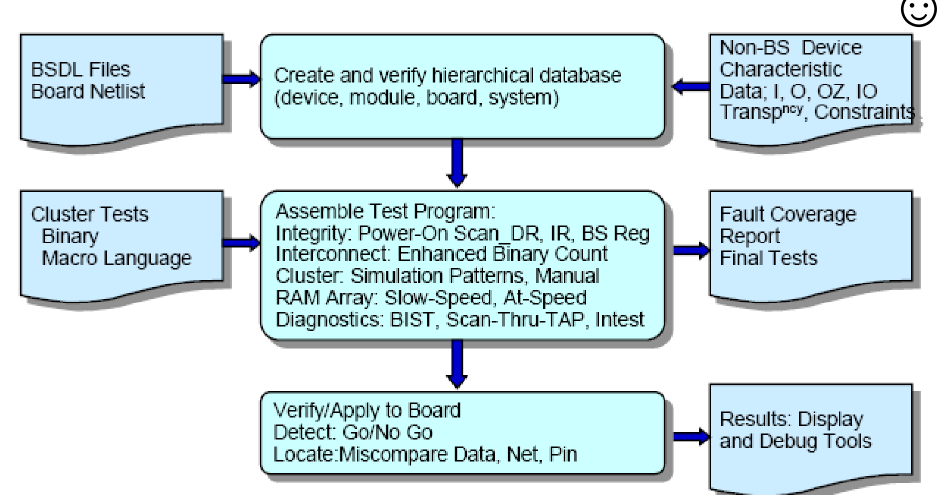


- ❑ Use ICT nails to access uncontrollable/unobservable cluster-internal nets
- ❑ Select the real-nail locations on non-BS nets according to access to:
  - strategic disables for guarding or preventing bus conflicts.
  - buried nets in non-embraced clusters
  - other key control signals e.g. O_Enab, Bidir or 3-state control signals

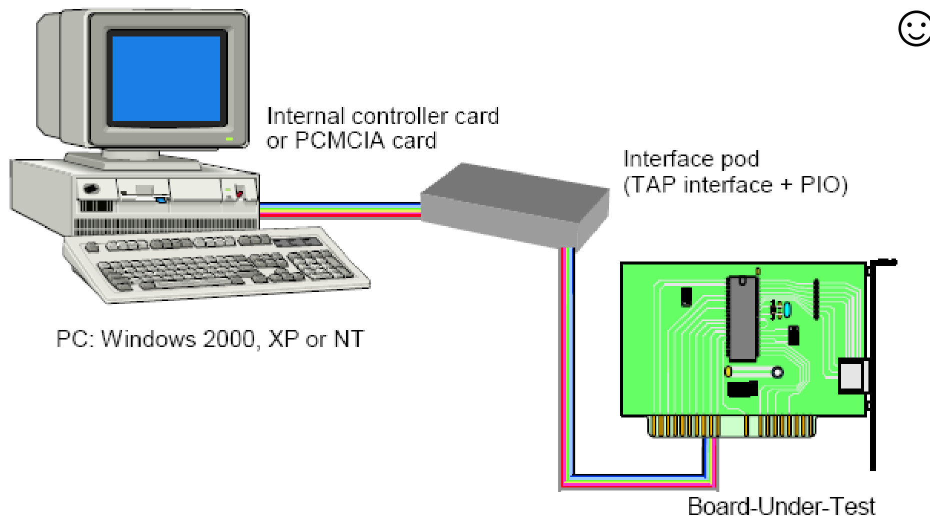
RAM Array Testing via Boundary Scan



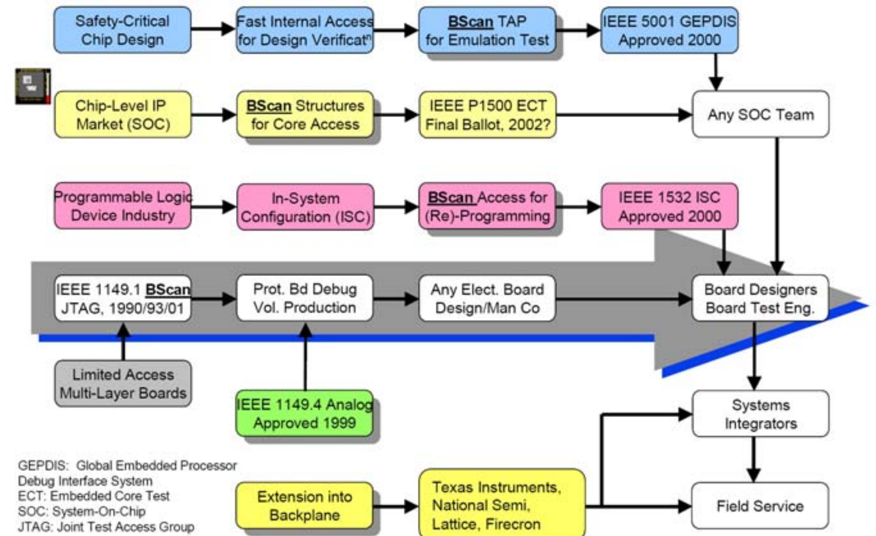
Tool Flow for Boundary Scan Tests



Hardware Requirement



Where are we today?



Spread of Design-for-Test (DFT)